S/N Unknown **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yong-Jun Hu	Examiner: Unknown
Serial No.:	Unknown	Group Art Unit: Unknown
Filed:	Herewith	Docket: 303.098US4
Title:	LOW ANGLE, LOW ENERGY PHYSICAL VAPOR DEPOSITION OF ALLOYS	

PRELIMINARY AMENDMENT

Box Patent Application
Commissioner for Patents
Washington, D.C. 20231

When the above-identified patent application is taken up for consideration, please amend the application as follows:

In the Specification

On page 1, under the title, please add the following paragraph:

—This application is a divisional of U.S. Serial No. 09/139,583 filed August 25, 1998, which is a continuation of U.S. Serial No. 08/964,575 filed November 5, 1997, now U.S. Patent 5,863,393, which is a divisional of U.S. Serial No. 08/677,659 filed July 8, 1996, now U.S. Patent 5,725,739. —

Please substitute the following paragraph that begins on Page 1, line 19 and ends on Page 2, line 5 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

One way in which circuit resistance is decreased is by creating low-resistance, ohmic contacts at the device level. Ohmic contacts exhibit nearly linear current-voltage characteristics in both directions of current flow. Various factors affect the type of contact which is maintained. Increasing dopant concentration in the semiconductor contact area decreases contact resistance, up to the solubility of the dopant at the temperature at which it is introduced. Unclean semiconductor surfaces (i.e., those which contain a native oxide film) increase contact resistance. Native oxides are a problem due to silicon's rapid oxidation rate when exposed to an oxygen

ambient. The most widely used method for removal of such oxides is by dipping the wafer in a hydrofluoric acid solution. However, this does not [provide] perfect cleaning of the semiconductor substrate because some native oxide forms between the time of the hydrofluoric acid dip and the deposition of metal contacts. Sputter etching has been used in an attempt to alleviate this imperfection, but it falls short because more oxide is introduced onto the semiconductor substrate than is removed.

Please substitute the following paragraph that begins on Page 3, line 16 and ends on Page 3, line 22 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

A primary method for depositing films by PVD is sputtering. Sputtering is a method by which atoms on a target are displaced to a desired surface, where they form a thin film. One possible solution to the problem of over consumption of silicon in shallow junctions is to use a PVD process to deposit a metal/silicon alloy, like titanium silicide. When [the target material] the deposited material is an alloy, the target is generally a composite target consisting of two or more materials mechanically arranged in a selected ratio, to yield a film of the desired alloy composition.

Please substitute the following paragraph that begins on Page 4, line 12 and ends on Page 4, line 20 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

A recess feature is defined by an upper and a lower surface. An alloy is deposited in a recess feature of a semiconductor substrate by sputtering an alloy or composite target onto the semiconductor substrate to form a layer of deposited material on the upper surface. After a period of time, a negative bias voltage is applied to the substrate, initiating a resputtering scheme, which operates simultaneously with the sputtering step. The layer of deposited material is resputtered, to redeposit the layer of deposited material onto the lower surface as a first layer

of resputtered material having a different stoichiometry than that of the deposited material. The resulting recess has improved bottom step coverage, which results in improved ohmic contacts.

Please substitute the following paragraph that begins on Page 6, line 15 and ends on Page 6, line 25 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

In one embodiment of the invention, a collimated PVD setup is used to obtain a low grazing angle during resputtering. In a second embodiment of the invention, a long-throw process is used to obtain a low, grazing angle during resputtering. A long-throw process utilizes a non-collimated PVD [tool] apparatus. During a long-throw process, spacing between a target and substrate is so large that only a portion of target material, having a small trajectory angle, with respect to the normal direction of the target, can reach the bottom of a contact hole. Note that in the case of resputtering material overhang, the normal direction of the target (material overhang) is measured, extending radially into the contact hole, in the plane of the substrate. The resulting material deposition rate and bottom step coverage are improved using this embodiment, due to the low energy and low angle mechanisms described previously.

Please substitute the following paragraph that begins on Page 6, line 26 and ends on Page 7, line 5 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

In a further embodiment of the invention, a sputtering chamber ambient atmosphere comprises argon and a nitrogen concentration of between approximately 0.1 to 3.0 percent by volume. Furthermore, in yet [a further] another embodiment of the invention, the resputtering step is followed by resputtering of at least one layer of material with a different stoichiometry than that of the first resputtered material layer, to form a "graded" stoichiometry of material

deposited in the contact hole. Using a nitrogen ambient increases the ion-to-neutral ratio, which increases the resputtering rate. Therefore, the resulting material deposition rate and bottom step coverage are improved using this embodiment.

Please substitute the following paragraph that begins on Page 7, line 17 and ends on Page 7, line 18 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

[Figure 3 is] Figures 3a and 3b are a silicided contact hole formed in accordance with the method of the invention.

Please substitute the following paragraph that begins on Page 8, line 1 and ends on Page 8, line 4 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

Existing equipment, such as a Varian M2000 PVD [tool] apparatus, is utilized to accomplish better bottom step coverage. The invention does not require purchasing a new deposition [tool] system and training employees on how to use it, saving cost and time in fabricating contacts for semiconductor devices.

Please substitute the following paragraph that begins on Page 9, line 26 and ends on Page 10, line 7 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

A process window starts by introducing an inert gas, such as argon, from a gas inlet (not shown here), through region 222 and into the space between the target 236 and substrate 200 to form a plasma 240, and allowing it to stabilize (approximately 5 to 10 seconds), as shown in Figure 2. Placing the gas under low, sub-atmospheric pressure creates the plasma (i.e., a mixture of positively charged gas ions and free electrons). A large negative voltage is then applied to the

target 236, directing the plasma ions 240 to the target 236 and sputtering it, for a period of time, allowing a steady-state to be reached. This time depends on the aspect ratio of the hole and actual [dimension] dimensions of the hole. For example, a contact hole of aspect ratio 4, with a 0.5 micron opening needs 5 seconds to reach this steady-state. However, a time frame of between approximately 0 to 25 seconds may be required, depending on geometries and setup of the PVD tool.

Please substitute the following paragraph that begins on Page 11, line 10 and ends on Page 11, line 26 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

In addition, after a subsequent annealing step, such preferential resputtering further decreases the resistivity of the contact, and prevents degradation of device performance by reducing native oxides. The [anneal] annealing step is performed in a furnace at temperatures of approximately 550 to 850 degrees Celsius, or by using rapid thermal processing (RTP) techniques. Corners of recesses are particularly adversely affected by the presence of remaining native oxides, which degrades device performance. Thus, depositing titanium-rich titanium silicide 154 in these corners 152, as shown in Figure 1a, improves bottom step coverage and removes native oxides, due to titanium's ability to react with such oxides to reduce them to titanium oxide and titanium silicide. The oxide layer remains on top of the silicide layer after annealing, separated from the underlying silicon. Prior art techniques have not accomplished this preferential resputtering of titanium silicide to allow native oxide reduction in bottom corners of contact holes. Typically, titanium silicide having the stoichiometry of approximately $TiSi_{1.8}$ is adequate to effectively reduce remaining native oxide. In general, between 30 to 50 angstroms of titanium can reduce approximately 12 angstroms of native oxide. This enhances reliable low contact resistance and provides a low defect density at the silicide/silicon interface 116.

Please substitute the following paragraph that begins on Page 11, line 27 and ends on Page 12, line 6 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

The exact details of the resputter scheme depend upon at least the type of device being manufactured (and, thus the particular electronic feature being fabricated), the aspect ratio of the hole, the depth (in absolute scale) of the hole, and the desired uniformity of the thin film. As for the [latter most] lattermost factor, [uniformities of] single metal thin films deposited by conventional techniques are approximately 50% uniform, but it is believed that the uniformity of thin films produced by the process of this invention can approach as little as a 10-20% deviation from complete uniformity without significant effort, and possibly even as low as a 2% deviation after a significant effort to optimize the process window.

Please substitute the following paragraph that begins on Page 12, line 7 and ends on Page 12, line 19 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

In a second embodiment of the invention, a long-throw PVD [setup] apparatus is used to obtain a low grazing angle during resputtering. A Varian M2000 PVD tool, or similar equipment well known to one skilled in the art, is used as shown in Figure 2. However, in this embodiment, the [tool] apparatus is noncollimated because a collimator 234 is not used. Instead of using a collimator, a low grazing angle is obtained due to the large substrate-to-target distance. The target 236 power is applied at less than approximately 18 kW. Higher target power provides for a higher deposition rate. The target power is adjusted, so that the desired deposition rate is obtained. A typical argon flow rate is 25 sccm. The target-to-substrate spacing is approximately 450 millimeters. In general, the target-to-substrate spacing is approximately 2 to 3 times greater than that utilized in a colllimated setup, and can range from between 100 to 1,000 millimeters, more or less, depending on the relative geometries of the PVD tool and substrate. The target-to-plasma spacing is adjusted, as is well known to one skilled in the art.

Please substitute the following paragraph that begins on Page 12, line 28 and ends on Page 13, line 16 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

After a steady-state is reached, a steady-state resputter scheme is started to redistribute material 150 overhang at the top corner 118 (upper surface) to the bottom corners (on the lower surface) of the contact hole 152, as shown in Figure 1a. The resputtered material 154 on the lower surface 116 of the contact hole 114 has a stoichiometry different than that of the deposited material 150 at the top corner 118, due to the differential resputtering rates of the alloy/composite constituent elements. This resputter scheme is initiated by varying the substrate 110 bias from voltage source 248. For example, using the current setup and contact hole 114 of aspect ratio 4, the zero bias is switched to a small bias (-15 to -65 Volts). In general, the substrate bias voltage should be less than the lowest sputtering threshold energy of any constituent of the alloy target. The amount of material 150 overhang is compensated with the amount of material 154 resputtered, providing a steady state process. The elements in the target material alloy, or composite, resputter at different rates, due to their different atomic masses, resulting in resputtered material <u>being</u> redistributed to the bottom of the contact hole, having a different stoichiometry than the deposited material on the upper surface of the contact hole. In general, heavier elements of a sputtered species sputter at a faster rate than lighter elements. The bias voltage is adjusted according to the elements present in the alloy or composite.

Please substitute the following paragraph that begins on Page 13, line 28 and ends on Page 14, line 15 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

In addition, after a subsequent [anneal] <u>annealing</u> step, such preferential resputtering decreases the resistivity of the contact, and prevents degradation of device performance by reducing native oxides. The [anneal] <u>annealing</u> step is performed in a furnace at temperatures of approximately 550 to 850 degrees Celsius, or <u>by</u> using rapid thermal processing (RTP)

techniques. Corners of recesses are particularly adversely affected by the presence of remaining native oxides, which degrades device performance. Thus, depositing titanium-rich titanium silicide 154 in these corners 152, as shown in Figure 1a, improves bottom step coverage and removes native oxides, due to titanium's ability to react with such oxides to form titanium oxide and titanium silicide upon subsequent annealing of the material. The oxide layer remains on top of the silicide layer after annealing, separated from the underlying silicon. Prior art techniques have not accomplished this preferential resputtering of titanium silicide to allow native oxide reduction in bottom corners of contact holes. Typically, titanium silicide having the stoichiometry of approximately $TiSi_{1.8}$ is adequate to effectively reduce any remaining native oxide. Typically, between 30 to 50 angstroms of titanium can completely reduce 12 angstroms of native oxide. This enhances reliable low contact resistance and provides a low defect density at the silicide/silicon interface 116.

Please substitute the following paragraph that begins on Page 14, line 16 and ends on Page 14, line 24 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

The exact details of the resputter scheme depend upon at least the type of device being manufactured (and, thus the particular electronic feature being fabricated), the aspect ratio of the hole, the depth (in absolute scale) of the hole, and the desired uniformity of the thin film. As for the [latter most] <u>lattermost</u> factor, [uniformities of] single metal thin films deposited by conventional techniques are approximately 50% uniform, but it is believed that the uniformity of thin films produced by the process of this invention can approach as little as a 10-20% deviation from complete uniformity without significant effort, and possibly even as low as a 2% deviation after a significant effort to optimize the process window.

Please substitute the following paragraph that begins on Page 15, line 3 and ends on Page 15, line 14 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

The maximum amount of silicon that is consumed from the substrate 310, as shown in [Figure 3] Figure 3a, is that needed to form titanium silicide in its equilibrium state. For example, titanium silicide has an equilibrium ratio of silicon to titanium of 2.0:1. When the resputtered material has a ratio of silicon to titanium of less than 2.0:1, silicon is consumed from the substrate to bring the ratio of silicon to titanium back to 2.0:1 after deposition. Compared to prior art techniques, since titanium silicide is being deposited instead of titanium, the profile of the substrate 310 does not change significantly during the process of forming a titanium silicide layer 354 thereon. The resulting layer of titanium silicide 354 provides lower contact resistance due to its generally planar shape. Although the resulting structure has been described in terms of a contact hole 314, deposited with titanium silicide 354, other types of materials and structures can be used, as described previously, without departing from the scope of the invention.

Please substitute the following paragraph that begins on Page 16, line 15 and ends on Page 16, line 22 of the Specification with the paragraph in the appendix entitled Clean Version of Specification Paragraphs. Specific amendments to this paragraph are detailed in the following marked-up paragraph:

In another embodiment, creating multiple layers of titanium silicides, with a stoichiometry, of $TiSi_x$, where $x > 2.0$, improves high temperature stability of titanium silicide by approximately 50 to 150 degrees Celsius, depending on how high a value of x device manufacturing processes can tolerate. However, when desired layers of resputtered material comprise a ratio of [titanium-to-silicon] silicon-to-titanium of greater than 2.0:1, the target material and layer of deposited material must have a ratio of [titanium-to-silicon] silicon-to-titanium of at least as great as that of the largest ratio of [titanium-to-silicon] silicon-to-titanium in the resputtered layers of material.

In the Claims

Cancel claims 1-30 without prejudice and add the following new claims 31-70:

31. A contact hole for a semiconductor device, comprising:

a bottom surface of a first material;

at least one vertical sidewall of a second material;

a generally planar layer of a third material covering the bottom surface, the third material including at least two different constituent elements.

32. The contact hole of claim 31 where the third material is an alloy or a composite.

33. The contact hole of claim 32 where the third material contains a refractory metal.

34. The contact hole of claim 32 where the third material is a silicide.

35. The contact hole of claim 32 where the third material is rich in titanium.

36. The contact hole of claim 32 where the stoichiometry of the third material is uniform.

37. The contact hole of claim 31 where the first material is silicon.

38. The contact hole of claim 37 where the third material consumes only a minimal amount of the silicon.

39. A contact hole for a semiconductor device, comprising:

a bottom surface of a first material;

at least one vertical sidewall of a second material and having a high aspect ratio;

a generally planar layer of a third material covering the bottom surface, the third material including at least two different constituent elements.

40. The contact hole of claim 39 where a height of the sidewall is at least four times a width of the bottom surface.

41. The contact hole of claim 39 where a width of the bottom surface is equal to or less than about 0.5 micron.

42. The contact hole of claim 39 where the third material is substantially confined to the bottom surface of the hole

43. A contact hole for a semiconductor device, comprising:

a bottom surface of a first material;

at least one vertical sidewall of a second material;

a layer of a third material covering the bottom surface with a thickness variation of less than 50%, the third material including at least two different constituent elements.

44. The contact hole of claim 43 where the thickness variation of the layer is less than about 20%.

45. The contact hole of claim 44 where the thickness variation of the layer is less than about 10%.

46. The contact hole of claim 43 where the planar layer contacts the sidewalls.

47. The contact hole of claim 46 where the planar layer does not extend a substantial distance up the sidewall from the bottom.

48. A contact hole for a semiconductor device, comprising:

a bottom surface of a first material;

at least one vertical sidewall of a second material;

a generally planar layer of a third material covering the bottom surface, the third material having a graded stoichiometery between two different elements.

49. The contact hole of claim 48 where the hole has a high aspect ratio.

50. The contact hole of claim 48 where the first material is silicon.

51. The contact hole of claim 48 where the second material is an insulator.

52. The contact hole of claim 48 where the planar layer contacts the sidewalls.

53. The contact hole of claim 52 where the third material is substantially confined to the bottom of the hole.

54. The contact hole of claim 48 where the third material is a silicide.

55. A contact hole for a semiconductor device, comprising:

a bottom surface of a first material;

at least one sidewall of an insulating material;

a generally planar layer of a third material covering the bottom surface, the third material including at least two different constituent elements.

56. The contact hole of claim 55 where the insulator is an oxide, a nitride, or a glass.

57. The contact hole of claim 55 where the layer of the third material does not extend substantially up the sidewall from the bottom.

58. The contact hole of claim 55 where the third material is a silicide.

59. An integrated circuit, comprising:

a substrate of a first material;

an insulator of a second material overlying the substrate;

multiple contact holes through the insulator to the substrate, each contact hole having at least one sidewall of the second material and a generally planar layer contacting the substrate, the layer including at least two different constituent elements.

60. The integrated circuit of claim 59 where the substrate is silicon.

61. The integrated circuit of claim 59 where the second material is an oxide, a nitride, or a glass.

62. The integrated circuit of claim 59 where the planar layer contacts the sidewalls.

63. The integrated circuit of claim 59 where the layer is planar within 50%.

64. The integrated circuit of claim 63 where the layer is planar within 20%.

65. An integrated circuit, comprising:

a substrate of a first material;

an insulator of a second material overlying the substrate;

multiple contact holes through the insulator to the substrate, each contact hole having at least one sidewall of the second material and a generally planar layer of a silicide contacting the substrate.

66. The integrated circuit of claim 65 where the silicide includes a refractory metal.

67. The integrated circuit of claim 66 where the refractory metal is titanium or cobalt.

68. The integrated circuit of claim 65 where the silicide has a uniform stoichiometry.

69. The integrated circuit of claim 65 where the silicide has at least two different stoichiometries.

70. The integrated circuit of claim 65 where the insulator has a top surface free of the silicide.

REMARKS

The modifications to the Specification numbered 2-6 and 8-22 above were previously entered in the parent patent application Serial No. 08/677,659 in response to an Examiner's Amendment to the Record, Paper #6, mailed September 29, 1997, by Examiner Aaron Weisstuch. The remaining modifications to the Specification represent typographical, grammatical, clerical or editorial modifications, and do not introduce new matter that would be prohibited by 35 USC 132.

The uniform stoichiometry recited in claims 36 and 68 is mentioned, inter alia, on page 7 line 25 of the Specification. Minimal consumption of the substrate by the material of the planar layer is discussed on page 15 line 1. Aspect ratios of the hole, specified in claims 39-41, are found on page 8 lines 11-14. Figs. 3a and 3b show the material in the layer at the bottom of the hole being confined thereto, and not extending substantially up the sidewalls, as recited in claims 42, 47, 53, and 57. Thickness variation of the bottom layer, as recited in claims 43-45 and 63-64, is described on page 14 lines 19-24. That the layer contacts the sidewalls, claims 46 and 52, is

found on line 29 of the same page. Different stoichiometries, recited in claims 48 and 69, is found on page 15 lines 19-28. The particular insulator materials of claims 56 and 61 are discussed on page 8 lines 10-11. Removal of the material deposited in the bottoms of the contact holes from other areas of the integrated circuit is mentioned on page 14 lines 25-27.

Respectfully submitted,

YONG-JUN HU

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6971

Date 5 April 2001 By _____
J. Michael Anglin
Reg. No. 24,916

"Express Mail" mailing label number: EL671639583US
Date of Deposit: April 5, 2001
This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box Patent Application, Washington, D.C. 20231.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 1, LINE 19 ENDING ON PAGE 2, LINE 5

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES
Applicant: Frankie Fariborz Roohparvar
Serial No.: 09/567,574

One way in which circuit resistance is decreased is by creating low-resistance, ohmic contacts at the device level. Ohmic contacts exhibit nearly linear current-voltage characteristics in both directions of current flow. Various factors affect the type of contact which is maintained. Increasing dopant concentration in the semiconductor contact area decreases contact resistance, up to the solubility of the dopant at the temperature at which it is introduced. Unclean semiconductor surfaces (i.e., those which contain a native oxide film) increase contact resistance. Native oxides are a problem due to silicon's rapid oxidation rate when exposed to an oxygen ambient. The most widely used method for removal of such oxides is by dipping the wafer in a hydrofluoric acid solution. However, this does not perfect cleaning of the semiconductor substrate because some native oxide forms between the time of the hydrofluoric acid dip and the deposition of metal contacts. Sputter etching has been used in an attempt to alleviate this imperfection, but it falls short because more oxide is introduced onto the semiconductor substrate than is removed.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
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Applicant: Frankie Fariborz Roohparvar
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A primary method for depositing films by PVD is sputtering. Sputtering is a method by which atoms on a target are displaced to a desired surface, where they form a thin film. One possible solution to the problem of over consumption of silicon in shallow junctions is to use a PVD process to deposit a metal/silicon alloy, like titanium silicide. When the deposited material is an alloy, the target is generally a composite target consisting of two or more materials mechanically arranged in a selected ratio, to yield a film of the desired alloy composition.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 4, LINE 12 ENDING ON PAGE 4, LINE 20

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES
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A recess feature is defined by an upper and a lower surface. An alloy is deposited in a recess feature of a semiconductor substrate by sputtering an alloy or composite target onto the semiconductor substrate to form a layer of deposited material on the upper surface. After a period of time, a negative bias voltage is applied to the substrate, initiating a resputtering scheme, which operates simultaneously with the sputtering step. The layer of deposited material is resputtered, to redeposit the layer of deposited material onto the lower surface as a first layer of resputtered material having a different stoichiometry than that of the deposited material. The resulting recess has improved bottom step coverage, which results in improved ohmic contacts.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 6, LINE 15 ENDING ON PAGE 6, LINE 25

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES
Applicant: Frankie Fariborz Roohparvar
Serial No.: 09/567,574

In one embodiment of the invention, a collimated PVD setup is used to obtain a low grazing angle during resputtering. In a second embodiment of the invention, a long-throw process is used to obtain a low, grazing angle during resputtering. A long-throw process utilizes a non-collimated PVD apparatus. During a long-throw process, spacing between a target and substrate is so large that only a portion of target material, having a small trajectory angle, with respect to the normal direction of the target, can reach the bottom of a contact hole. Note that in the case of resputtering material overhang, the normal direction of the target (material overhang) is measured, extending radially into the contact hole, in the plane of the substrate. The resulting material deposition rate and bottom step coverage are improved using this embodiment, due to the low energy and low angle mechanisms described previously.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 6, LINE 26 ENDING ON PAGE 7, LINE 5

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In a further embodiment of the invention, a sputtering chamber ambient atmosphere comprises argon and a nitrogen concentration of between approximately 0.1 to 3.0 percent by volume. Furthermore, in yet another embodiment of the invention, the resputtering step is followed by resputtering of at least one layer of material with a different stoichiometry than that of the first resputtered material layer, to form a "graded" stoichiometry of material deposited in the contact hole. Using a nitrogen ambient increases the ion-to-neutral ratio, which increases the resputtering rate. Therefore, the resulting material deposition rate and bottom step coverage are improved using this embodiment.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 7, LINE 17 ENDING ON PAGE 7, LINE 18

METHOD AND APPARATUS TO ACHIEVE FAST SUSPEND IN FLASH MEMORIES
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[Figure 3 is] Figures 3a and 3b are a silicided contact hole formed in accordance with the method of the invention.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 8, LINE 1 ENDING ON PAGE 8, LINE 4

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Existing equipment, such as a Varian M2000 PVD apparatus, is utilized to accomplish better bottom step coverage. The invention does not require purchasing a new deposition system and training employees on how to use it, saving cost and time in fabricating contacts for semiconductor devices.

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A process window starts by introducing an inert gas, such as argon, from a gas inlet (not shown here), through region 222 and into the space between the target 236 and substrate 200 to form a plasma 240, and allowing it to stabilize (approximately 5 to 10 seconds), as shown in Figure 2. Placing the gas under low, sub-atmospheric pressure creates the plasma (i.e., a mixture of positively charged gas ions and free electrons). A large negative voltage is then applied to the target 236, directing the plasma ions 240 to the target 236 and sputtering it, for a period of time, allowing a steady-state to be reached. This time depends on the aspect ratio of the hole and actual dimensions of the hole. For example, a contact hole of aspect ratio 4, with a 0.5 micron opening needs 5 seconds to reach this steady-state. However, a time frame of between approximately 0 to 25 seconds may be required, depending on geometries and setup of the PVD tool.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 11, LINE 10 ENDING ON PAGE 11, LINE 26

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In addition, after a subsequent annealing step, such preferential resputtering further decreases the resistivity of the contact, and prevents degradation of device performance by reducing native oxides. The annealing step is performed in a furnace at temperatures of approximately 550 to 850 degrees Celsius, or by using rapid thermal processing (RTP) techniques. Corners of recesses are particularly adversely affected by the presence of remaining native oxides, which degrades device performance. Thus, depositing titanium-rich titanium silicide 154 in these corners 152, as shown in Figure 1a, improves bottom step coverage and removes native oxides, due to titanium's ability to react with such oxides to reduce them to titanium oxide and titanium silicide. The oxide layer remains on top of the silicide layer after annealing, separated from the underlying silicon. Prior art techniques have not accomplished this preferential resputtering of titanium silicide to allow native oxide reduction in bottom corners of contact holes. Typically, titanium silicide having the stoichiometry of approximately $TiSi_{1.8}$ is adequate to effectively reduce remaining native oxide. In general, between 30 to 50 angstroms of titanium can reduce approximately 12 angstroms of native oxide. This enhances reliable low contact resistance and provides a low defect density at the silicide/silicon interface 116.

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Applicant: Frankie Fariborz Roohparvar
Serial No.: 09/567,574

The exact details of the resputter scheme depend upon at least the type of device being manufactured (and, thus the particular electronic feature being fabricated), the aspect ratio of the hole, the depth (in absolute scale) of the hole, and the desired uniformity of the thin film. As for the lattermost factor, single metal thin films deposited by conventional techniques are approximately 50% uniform, but it is believed that the uniformity of thin films produced by the process of this invention can approach as little as a 10-20% deviation from complete uniformity without significant effort, and possibly even as low as a 2% deviation after a significant effort to optimize the process window.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
BEGINNING ON PAGE 12, LINE 7 ENDING ON PAGE 12, LINE 19

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In a second embodiment of the invention, a long-throw PVD apparatus is used to obtain a low grazing angle during resputtering. A Varian M2000 PVD tool, or similar equipment well known to one skilled in the art, is used as shown in Figure 2. However, in this embodiment, the apparatus is noncollimated because a collimator 234 is not used. Instead of using a collimator, a low grazing angle is obtained due to the large substrate-to-target distance. The target 236 power is applied at less than approximately 18 kW. Higher target power provides for a higher deposition rate. The target power is adjusted, so that the desired deposition rate is obtained. A typical argon flow rate is 25 sccm. The target-to-substrate spacing is approximately 450 millimeters. In general, the target-to-substrate spacing is approximately 2 to 3 times greater than that utilized in a colllimated setup, and can range from between 100 to 1,000 millimeters, more or less, depending on the relative geometries of the PVD tool and substrate. The target-to-plasma spacing is adjusted, as is well known to one skilled in the art.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
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After a steady-state is reached, a steady-state resputter scheme is started to redistribute material 150 overhang at the top corner 118 (upper surface) to the bottom corners (on the lower surface) of the contact hole 152, as shown in Figure 1a. The resputtered material 154 on the lower surface 116 of the contact hole 114 has a stoichiometry different than that of the deposited material 150 at the top corner 118, due to the differential resputtering rates of the alloy/composite constituent elements. This resputter scheme is initiated by varying the substrate 110 bias from voltage source 248. For example, using the current setup and contact hole 114 of aspect ratio 4, the zero bias is switched to a small bias (-15 to -65 Volts). In general, the substrate bias voltage should be less than the lowest sputtering threshold energy of any constituent of the alloy target. The amount of material 150 overhang is compensated with the amount of material 154 resputtered, providing a steady state process. The elements in the target material alloy, or composite, resputter at different rates, due to their different atomic masses, resulting in resputtered material being redistributed to the bottom of the contact hole, having a different stoichiometry than the deposited material on the upper surface of the contact hole. In general, heavier elements of a sputtered species sputter at a faster rate than lighter elements. The bias voltage is adjusted according to the elements present in the alloy or composite.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
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In addition, after a subsequent annealing step, such preferential resputtering decreases the resistivity of the contact, and prevents degradation of device performance by reducing native oxides. The annealing step is performed in a furnace at temperatures of approximately 550 to 850 degrees Celsius, or by using rapid thermal processing (RTP) techniques. Corners of recesses are particularly adversely affected by the presence of remaining native oxides, which degrades device performance. Thus, depositing titanium-rich titanium silicide 154 in these corners 152, as shown in Figure 1a, improves bottom step coverage and removes native oxides, due to titanium's ability to react with such oxides to form titanium oxide and titanium silicide upon subsequent annealing of the material. The oxide layer remains on top of the silicide layer after annealing, separated from the underlying silicon. Prior art techniques have not accomplished this preferential resputtering of titanium silicide to allow native oxide reduction in bottom corners of contact holes. Typically, titanium silicide having the stoichiometry of approximately $TiSi_{1.8}$ is adequate to effectively reduce any remaining native oxide. Typically, between 30 to 50 angstroms of titanium can completely reduce 12 angstroms of native oxide. This enhances reliable low contact resistance and provides a low defect density at the silicide/silicon interface 116.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
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The exact details of the resputter scheme depend upon at least the type of device being manufactured (and, thus the particular electronic feature being fabricated), the aspect ratio of the hole, the depth (in absolute scale) of the hole, and the desired uniformity of the thin film. As for the lattermost factor, single metal thin films deposited by conventional techniques are approximately 50% uniform, but it is believed that the uniformity of thin films produced by the process of this invention can approach as little as a 10-20% deviation from complete uniformity without significant effort, and possibly even as low as a 2% deviation after a significant effort to optimize the process window.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
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The maximum amount of silicon that is consumed from the substrate 310, as shown in Figure 3a, is that needed to form titanium silicide in its equilibrium state. For example, titanium silicide has an equilibrium ratio of silicon to titanium of 2.0:1. When the resputtered material has a ratio of silicon to titanium of less than 2.0:1, silicon is consumed from the substrate to bring the ratio of silicon to titanium back to 2.0:1 after deposition. Compared to prior art techniques, since titanium silicide is being deposited instead of titanium, the profile of the substrate 310 does not change significantly during the process of forming a titanium silicide layer 354 thereon. The resulting layer of titanium silicide 354 provides lower contact resistance due to its generally planar shape. Although the resulting structure has been described in terms of a contact hole 314, deposited with titanium silicide 354, other types of materials and structures can be used, as described previously, without departing from the scope of the invention.

CLEAN VERSION OF SPECIFICATION PARAGRAPH
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In another embodiment, creating multiple layers of titanium silicides, with a stoichiometry, of $TiSi_x$, where $x > 2.0$, improves high temperature stability of titanium silicide by approximately 50 to 150 degrees Celsius, depending on how high a value of x device manufacturing processes can tolerate. However, when desired layers of resputtered material comprise a ratio of silicon-to-titanium of greater than 2.0:1, the target material and layer of deposited material must have a ratio of silicon-to-titanium of at least as great as that of the largest ratio of silicon-to-titanium in the resputtered layers of material.